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Comparative Study Of Different Voltage Controlled Oscillator Using CMOS Technology

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Abstract

Oscillators are integral part of many electronic systems. An oscillator is an electronic device used for the purpose of generating a signal. Most electronic signal processing systems require frequency or time reference signals. This paper deals with the analysis and design of CMOS oscillators more specifically voltage controlled oscillators (VCOs).Voltage Controlled Oscillator is an electronic oscillator whose output frequency is controlled by a voltage input.VCO can be built using many circuit techniques. Primarily, there are two methods of designing CMOS VCOs, one uses a ring oscillator and other uses a Schmitt trigger. Though there are so many design requirements of a VCO, which are phase stability, large electrical tuning range, linearity of frequency verses control voltage, large gain factor, capability of accepting wideband modulation and low cost but the most important factor in designing the VCO is the linearity, on the basis of which the comparison between CMOS VCOs is described. With respect to digital phones that use these circuits, low power consumption, small size, and leakage current and low fabrication costs are important design factors. In this paper main objective is to reduce the leakage current, voltage and power consumption. It is observed by the parameters calculated.

Keywords: *Leakage current, Average Power, Ring oscillator, Voltage Controlled Oscillator.*

1. Introduction

The crystal oscillator, mainly, cannot generate a frequency up to 100MHz, so it makes use of off-chip as the reference signal. In the chip, a Voltage Controlled Oscillator is applied to give the higher frequency periodic signal for the systems [1]. One of the causes that VCO is a usually utilized circuit is that it is a fundamental component of a PLL. PLL finds expansive applications in many areas such as communication systems, wireless systems, digital circuits and power systems [2]. It is to compose an output signal which oscillates at the similar frequency as the input signal. When the Phase Locked Loop is in lock, it acts as follows: The phase detector develops an output whose direct current value is proportional to the phase difference in middle of the input periodic signal which arranges the oscillator output [3]. The low pass filters than reduce the high frequency change in the phase detector output because the VCO input signal is direct current and this restricts the oscillation frequency of the VCO equal to that of the input signal [4]. At one time lock, Phase Locked Loop tracks the input frequency because of little variation. In this case the phase difference in middle of the input signal and the VCO output will enhance, due to the fact the direct current output of the phase detector and low pass filter will increase and the frequency of the input signal will also expand [5]. For that reason, the frequency will rise to save the increase in the frequency of the input and its VCO of the input will also soar. It is realized that the Voltage Controlled Oscillator frequency will increment at the end of the accurate number and then reduce to the desired value [6]. As the loop won‘t retake close up to the Voltage Controlled Oscillator frequency similar to the input frequency thus the static phase inaccuracy is put into order to its proper value [7].

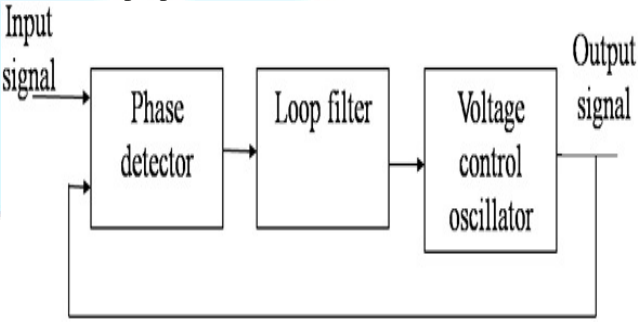

Figure1.1 Phase Locked Loop using VCO

The example shows that the frequency band restrains the choice of the reference frequency. Generally, as the reference frequency is equivalent to the operation frequency of the Phase Detector (PD) and the charge pump of the PLL, a wide frequency range will desire the Phase Detector and charge pump to work at a higher frequency,

which necessitates larger power consumption [8]. The two high frequency blocks in PLL, namely the Voltage-Controlled Oscillator (VCO) and the Current Controlled Oscillator are most essential in the feasibility of integration in a CMOS process [9]. But in this thesis, main topic is Voltage Controlled Oscillator, so we briefly describe it.

In Voltage Controlled Oscillator (VCO),let us discuss oscillator. The first electronic oscillating was constructed by Elihu Thomson in 1892 [10]. Oscillators are circuits that produce an output signal at a certain frequency with DC power supply as it transforms direct current from a power supply to an alternating current signal. Oscillators are extensively applied in different electronic devices [11].Clock signals that regulate quartz clocks and computer but oscillators contain signals broadcast by radio and television transmitters and sounds produced by electronic beepers and video games [12]. An oscillator must accommodate amplification and the output is feedback to sustain the input. Abundant power must be feedback to the input for the oscillator to control itself as in occurrence of signal generator. The oscillator is self-controlled, since the feedback signal is regenerative i.e. positive feedback [13].

2. Proposed Design

Different leakage reductions Technique are being applied in the VCO circuit for lowering the leakage power and leakage current in the circuit for enhancing the performance in the circuit. Different VCO circuits designed in this paper are following.

2.1 Ring oscillator VCO using CMOS

Ring Oscillator based VCO circuit consists of 2 stages. The former one is the input stage and the later one is the Ring Oscillator circuit as shown in Fig.4.1. Ring oscillator circuit consists of five inverter circuits joined in series. This circuit is known as current starved type VCO circuit. The inverter circuit in the Ring Oscillator consists of complimentary pair of transistors which function as a current source in the circuit. Current source in the circuit helps in controlling and limiting the current that is being supplied to the inverter. Current mirror in the circuit helps in controlling the current starved in the circuit and also delay in the circuit designed. Input stage of VCO circuit has high input impedance. It comprises of an additional pair of transistor added in the beginning of the circuit. The frequency of the circuit is defined as the time taken by the circuit for charging and discharging of the capacitance at each inverter stage in the circuit. During transition, charging and discharging of the circuit takes place, thus the total capacitance is the sum of both input and output capacitance of the circuit. The DC voltage helps in controlling the operating frequency of the VCO which further adjusts the current after each inverter stage in the circuit

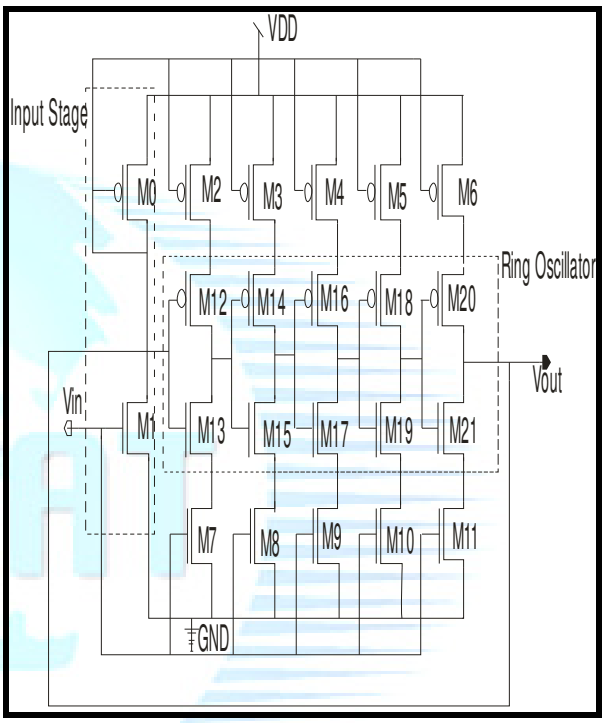

Figure 2.1 VCO using Ring Oscillator.

2.2 MTCMOS in Ring Oscillator VCO

For minimizing leakage in the circuit, various techniques are being introduced. One of the technique is MTCMOS. MTCMOS stands for "Multiple-Threshold CMOS". A high threshold PMOS and high threshold NMOS are introduced in the circuit at the place of VDD and GND respectively. The source terminal of the high threshold PMOS and NMOS is connected to the actual VDD and GND terminal of the circuit respectively. The drain terminal of the PMOS and NMOS will act as virtual VDD and virtual GND for the circuit. Leakage power in the circuit is reduced using the higher threshold transistor in place of actual VDD and GND, thus enhancing the performance of the circuit. The supply voltage for the PMOS is 0 V and for the NMOS is 0.7 V. The main drawback of this technique is the sizing of the sleep transistor. MTCMOS in VCO is shown in Figure 1.3.

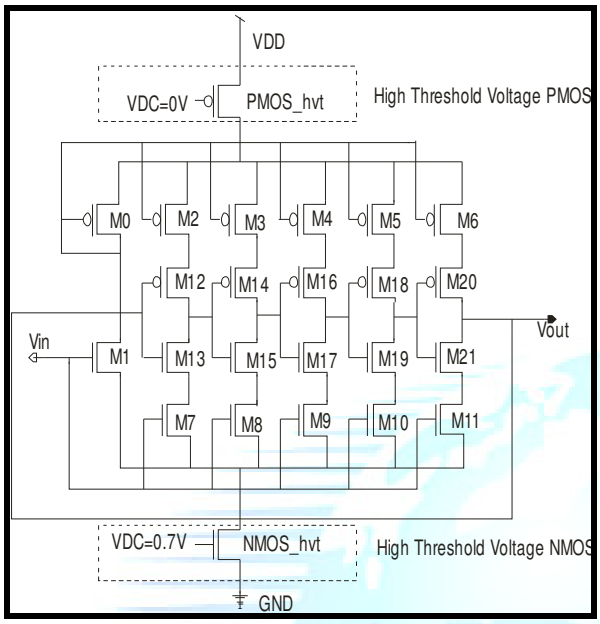

Figure 2.2 MTCMOS Technique in VCO using Ring Oscillator

2.3 AVL Technique in Ring Oscillator VCO

AVL stands for "Adaptive Voltage Level" technique. VCO circuit using AVL is displayed in Fig.4.5. It is of two types likewise SVL i.e., AVL-G and AVL-S. AVL-G is the technique when the additional sleep transistor is connected at the ground terminal, while AVL-S is the technique when the sleep transistor is connected to the supply.

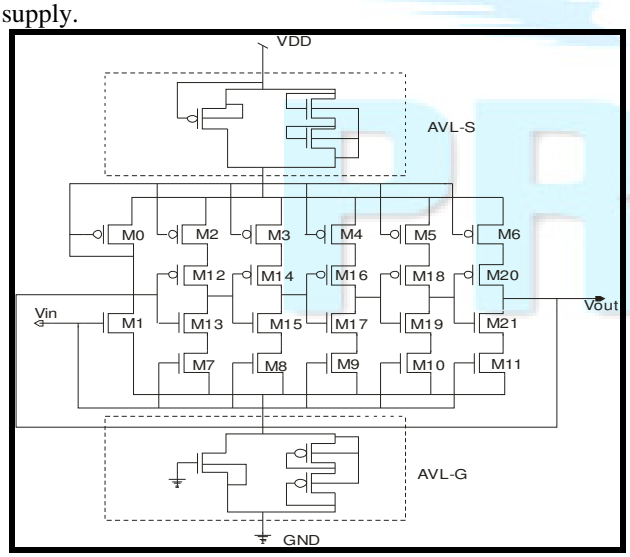

Figure 2.3 AVL in VCO using Ring Oscillator

Both the techniques are being applied in the circuit to enhance the performance of the circuit. AVL-G leads to increase in ground level in the circuit when the circuit is in active mode. It leads to decrease in the leakage current when the circuit is in standby or cutoff mode. AVL-S technique helps in curtailing the gate leakage current in the circuit.

3. Simulation Result

The proposed FinFET based Voltage Controlled Oscillator (VCO) has been designed using the cadence virtuoso tool of IC 6.1 version and the simulations are performed using the 45nm technology. The different values used for simulation were supply voltage = 0.7V, capacitance = 1µf and temperature = 27ºC. The simulation result of different technique based Voltage Controlled Oscillator with different power is shown below in the Table 1.1.

Parameters	Simple VCO	MTCMOS based VCO	AVL based VCO
Average Power(in Watts)	84.12nw	64.42nW	36.02nW
Leakage Current(in Ampere)	10.64pA	7.69pA	8.34 nA

Table 3.1 Different Technique based Voltage Controlled Oscillator

3.1 Parameters of simple VCO

The functionality of the Voltage Controlled Oscillator using FinFET is defined by the simulation result.

3.1.1 Transient Response

The transient response shows the response of a system in the form of output by giving different input to it.

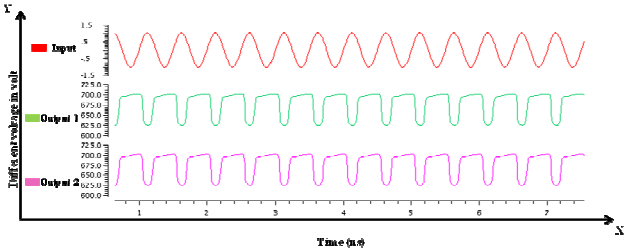

Figure 3.1 Transient Response of Voltage Controlled Oscillator

Figure 3.1 indicates input/output waveform of Voltage Controlled Oscillator with the help of cadence virtuoso tool with schematic result analysis.

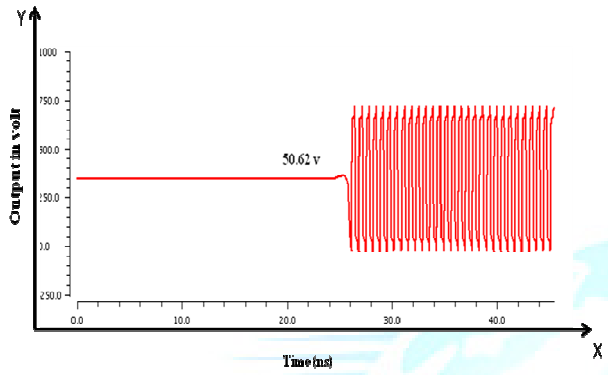

Figure 3.2 Transient Response of Ring Oscillator

Figure 3.2 indicates output waveform of Ring Oscillator with the help of cadence virtuoso tool.

3.1.2 Leakage Current

Leakage current of the Ring Oscillator is estimated during the standby mode. To calculate the leakage current of the current starved VCO, NMOS transistor is desired to measure the leakage current that is connected at the pull down network below the whole circuit. Sleep transistor is OFF for this technique whenever leakage current calculation is estimated. Leakage current is derived by the equation given below

$$P_{Leakage}=I_{Leakage}.V_{DD}$$

The leakage current versus time graph is shown in Figure 3.3. The calculate leakage current is 1.64pA.

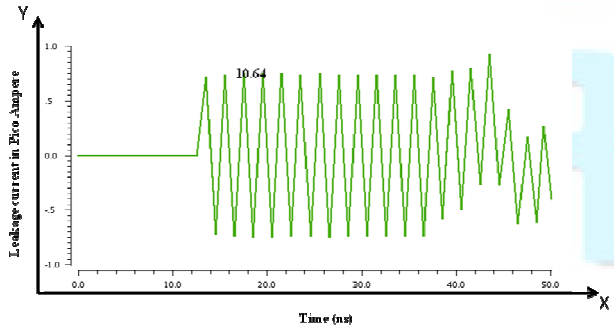

Figure 3.3 Leakage Current versus Time Graph

3.1.3 Average Power

The average power is also calculated. The average power dissipation happens due to the static and dynamic power dissipation and the unit of power is watt. It needs battery power consumption and is linked to the cooling. The average power is calculated as 16.71nW.

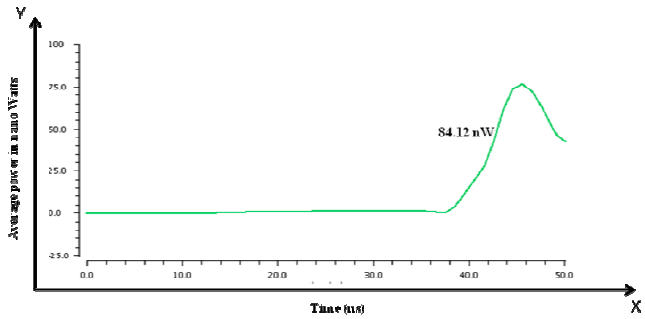

Figure 3.4 Average Power versus Time Graph

3.2 Parameters of MTCMOS based VCO

3.2.1 Transient Response

The transient response shows the response of a system in the form of output by giving different input to it.

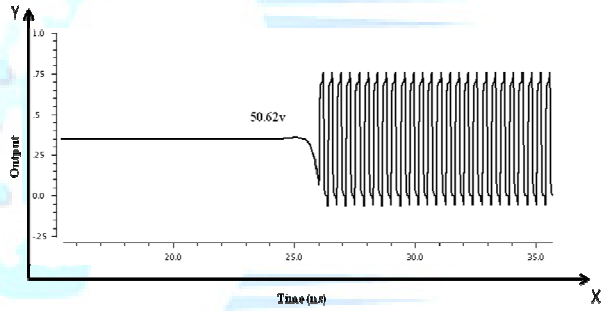

Figure 3.5 Transient Response of Ring Oscillator

Figure 3.5 indicates input/output waveform of Voltage Controlled Oscillator with the help of cadence virtuoso tool with schematic result analysis.

3.2.2 Leakage Current

For the design of Voltage Controlled Oscillator, it calculates 7.49pA. The leakage current versus time graph is illustrated in figure 3.6.

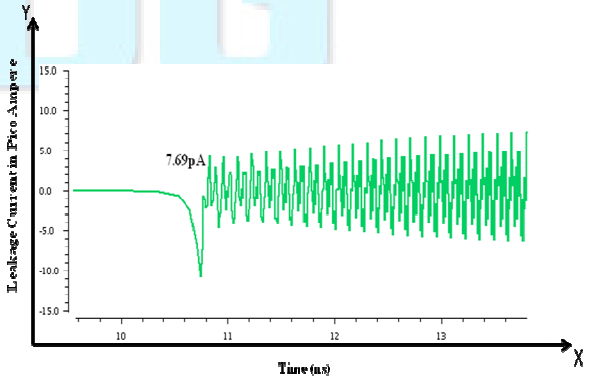

Figure 3.6 Leakage Current versus Time Graph MTCMOS based VCO

3.2.3 Average Power

The graph of average power of VCO using MTCMOS technique is shown in Figure 3.7. It helps us to read the values of the parameters that are calculated with the CADENCE virtuoso tool.

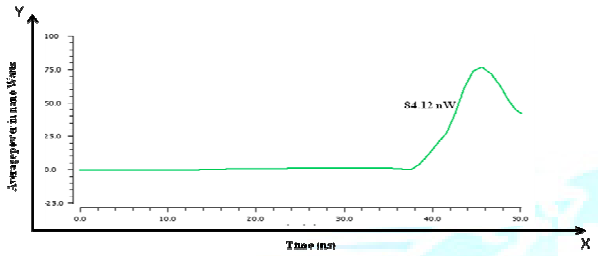

Figure 3.7 Average Power versus Time Graph MTCMOS based VCO

3.3 PARAMETER OF AVL BASED VCO

3.3.1 Transient Response

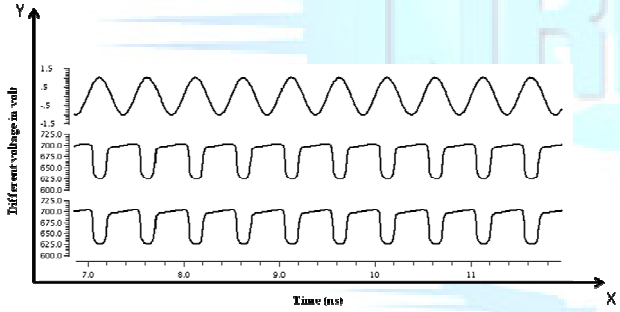

Figure 3.8 Transient Response of Voltage Controlled Oscillator

The transient response shows the response of a system in the form of output by giving different input to the circuit. It helps us to read the values of the parameters that are calculated with the CADENCE virtuoso tool.

3.3.2 Leakage Current

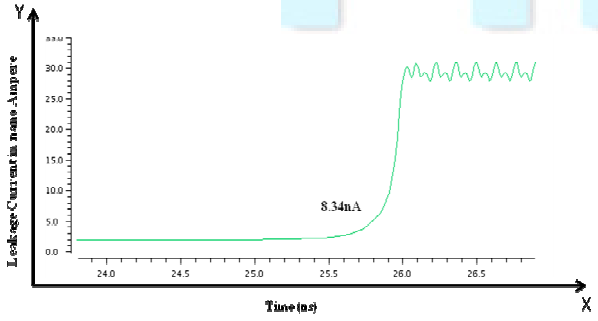

Figure 3.9 Leakage Current versus Time Graph Using AVL Technique

For the design of Voltage Controlled Oscillator, it calculates 5.18pA. The leakage current versus time graph is exhibited in figure 3.9.

3.3.3 Average Power

The graph of average power of VCO using AVL technique is illustrated in Figure 3.10. It helps us to read the values of the parameters that are calculated using the CADENCE virtuoso tool.

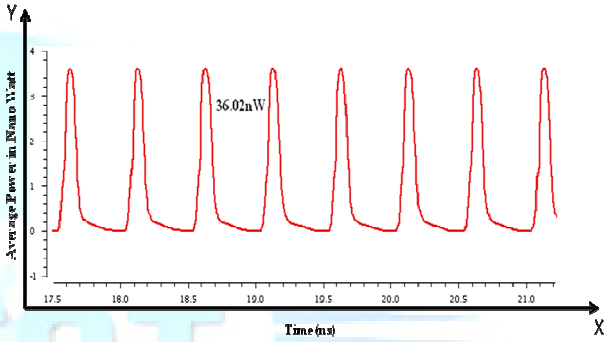

Figure 3.10 Average Power versus Time Graph using AVL Technique

4. Conclusions

. With the help of the leakage reduction technique in the VCO Circuit, a vast enhancement in the performance of the circuit is observed.The average power in the circuit is changed from 84.12nw in CMOS based to 64.42nw,36.02nw using MTCMOS and AVL technique respectively. The leakage current in the circuit is changed from 10.64 pA in CMOS based to 7.69pA,8.34nA using MTCMOS and AVL technique respectively.

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